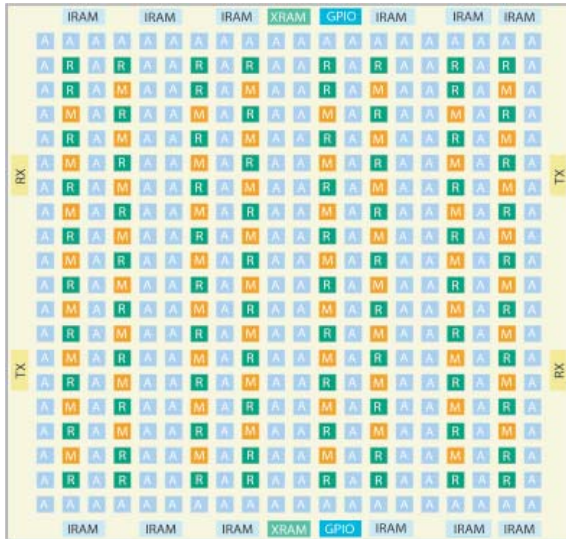




### FPOA Overview

The Arrix® Family of Field Programmable Objects Arrays is the second generation of FPOA products from MathStar. A 1 GHz FPOA delivers up to four times the performance of today's top FPGAs and combines high performance and re-programmability to meet a wide variety of application needs. FPOAs are comprised of hundreds of objects that pass data and signals to each other through a patented 1 GHz interconnect fabric. The Arrix Family of FPOAs support 256 Arithmetic Logic Unit (ALU), 80 Register File, and 64 MAC (multiply accumulator) objects. The objects and the interconnect fabric run on a common clock and operate deterministically at frequencies up to 1 GHz. This deterministic performance eliminates the tedious timing closure steps associated with FPGAs, reducing design iterations and development time.



- A Arithmetic Logic Units
- R Register Files
- M Multiply/Accumulators
- IRAM Internal SRAM Banks
- XRAM External Memory Interfaces
- GPIO General Purpose I/O Banks
- TX High Speed Transmit Ports
- RX High Speed Receive Ports

### Features and Benefits

Features	Description and Benefits
High Performance	1 GHz operation / 1 GHz data movement - up to four times faster than today's high end FPGAs
Deterministic, cycle-based timing closure	Objects and interconnect fabric run deterministically on a common clock. Designs meet targeted performance.
Re-programmability	Re-programmable in as little as 10 milliseconds - delivers on the fly flexibility in the field.
Simplified Design Flow	Deterministic, cycle based timing closure, graphical design environment, and rapid floorplanning and placement speed time to market.

### Arrix Family Silicon Object and I/O

Resources	Number	Operating Speed	Size Each	Total Capacity
ALU	256 objects	Up to 1 GHz	16 bits + control logic	One operation per clock
RF	80 objects	Up to 1 GHz	128 Byte + 80 tag bits	One operation per clock
MAC	64 objects	Up to 1 GHz	16x16 bit multiplier	One operation per clock
Internal RAM	12 banks	Up to 500 MHz	2K x 76 bits	57 GBytes/sec total
External RAM	2 interfaces	Up to 300 MHz	36 bit RLDRAM II	5.4 GBytes/sec total
GPIO	2 banks	Up to 100 MHz	48 pins per bank	96 pins
High Speed I/O Transmits	2 ports	18-500 MHz DDR	16 + 1 bit LVDS	32 Gbps output
High Speed I/O Receive	2 ports	250-500 MHz DDR	16 + 1 bit LVDS	32 Gbps input

**Array Objects - Programming Features**

**A Arithmetic Logic Unit (ALU)**

16 bit data path  
 4 fully programmable control bits  
 8 instruction state machine per ALU  
 Each state programmable with over 32 instructions  
 (Add/Sub, shift/rotate, AND/OR/XOR, etc.)

**R Register File (RF)**

Configurable to 64 entries of 16 + 4 bit data or 32 entries of 32 + 8 bit data  
 Three operational modes

- Dual ported RAM
- Single-cycle, dual-ported FIFO
- Single-cycle Read Sequential/Write Random

**M Multiply Accumulator (MAC)**

16 x 16 single cycle throughput multiplier  
 32 bit intermediate result, signed or unsigned  
 40 bit accumulator, 256 MACs before overflow

**IRAM Internal RAM**

12 independent blocks of 19 KB each  
 Each block is 2K deep and 76 bits wide  
 Single cycle access up to 500 MHz  
 Two cycle access up to 1 GHz  
 228 KB maximum memory size

**Periphery Objects - Programming Features**

**XRAM External RAM**

2 Independent RLD RAM II memory controllers  
 Each controller runs up to 300 MHz DDR  
 Each controller is 36 bits wide  
 144 MB maximum memory size per interface  
 2.7 GB/s maximum throughput per interface

**TX High Speed Transmit ports**

Two independent transmit interfaces  
 16+1 or 8+1 bit width configuration  
 Operation from 18 MHz to 500 MHz DDR  
 Operation up to 640 MHz SDR  
 Up to 16 Gbps data throughput per interface

**RX High Speed Receive ports**

Two independent receive interfaces  
 16+1 or 8+1 bit width configuration  
 Operation from 250 MHz to 500 MHz DDR  
 Operation up to 640 MHz SDR  
 Up to 16 Gbps data throughput per interface

**GPIO General Purpose I/O**

96 pins total - 2 banks of 48 pins each  
 Operation up to 100 MHz SDR  
 LVCMOS: 2.5 V and 3.3 V tolerant  
 Highly programmable clocking - internal, external or asynchronous

**Packaging - Environmental Specifications**

Operating Parameter	Minimum	Nominal	Maximum
Voltage*	1.14 V	1.2 V	1.26 V
Junction Temperature*	-40° C	n/a	125° C
Package Size	n/a	31 x 31 mm	n/a

\* Voltage tolerance and junction temperatures vary across speed grades. Consult Arrix Family data sheet for details.

**Arrix Product Family Ordering**

Maximum Operating Frequency	Product Code	Package
1 GHz	MOA2400D-10R*	HFCBGA-896
900 MHz	MOA2400D-09R*	HFCBGA-896
800 MHz	MOA2400D-08R*	HFCBGA-896
600 MHz	MOA2400D-06R*	HFCBGA-896

\* Available in RoHS and Eutectic packages.

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