

**April 2008****Product Brief**

Features

- Decodes at rates up to 200 Mbps
- Self-configures to different video modes based on incoming stream
- Decodes 8 SD MPEG-2 bitstreams of MP@ML (4:2:0 format) with up to 25 Mbps per channel
- Decodes 4 SD MPEG-2 bitstreams of 422P@ML (4:2:2 format) with up to 50 Mbps per channel
- Decodes 6 SD MPEG-2 bitstreams of 422P@ML (4:2:2 format) with up to 25 Mbps per channel
- Decodes 1 HD MPEG-2 bitstream of MP@HL (1080i or 720p, 4:2:0 or 4:2:2 format) up to 200 Mbps
- Outputs video compatible with the ITU-R BT.601 (4:2:2) format
- Designed to meet ISO/IEC 13818-2 requirements
- For use with Arrix™ MOA2400D-08 FPOA

Applications

- Professional video
- Security surveillance with compressed video
- Multi-display applications
- Video hardware acceleration

Arrix FPOA Overview

The MathStar Field-Programmable Object Array (FPOA) architecture comprises an array of silicon objects, each performing a specific function at data rates up to 1 GHz. The architecture supports three kinds of 16-bit core objects: an Arithmetic Logic Unit (ALU), a Multiply-Accumulator (MAC) and a Register File (RF). The objects are interconnected by a two-tier interconnect structure. The interconnect structure allows for 1 GHz connectivity between Nearest Neighbor connections as well as 1 GHz connectivity between non-adjacent objects through patented Party Line interconnects. These objects are coupled with

distributed internal RAM (IRAM), dedicated external memory controllers (XRAM) and a wide range of high-speed and general-purpose I/O (GPIO) to form the complete FPOA architecture. Because of its high performance, an FPOA can run many applications up to four times faster than top FPGA architectures.

General Description

The MPEG-2 Multi-stream Decoder for FPOA core can be used to implement ISO/IEC 13818-2 compliant systems. The core is capable of decoding up to eight SD channels of MPEG-2 video or one HD channel in real-time.

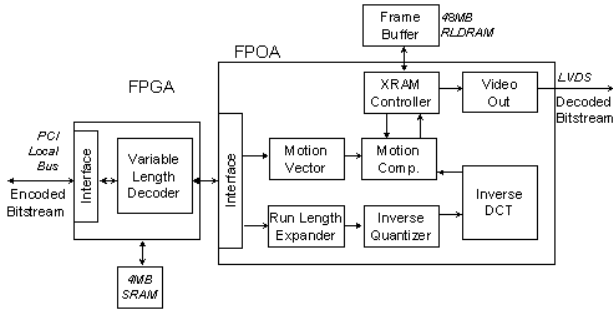
This decoder accepts input data streams and control/status commands through a PCI J-mode Local Bus and performs the following operations:

- Processing of compressed bitstreams to re-build live video sequences
- External host provides the encoded bitstream with channel information embedded in the data header
- Depending on the profile and level the decoder can handle various bitstream rates and picture sizes
- The decoder uses 48MB of RLDRAM to store reconstructed pictures and 4MB of SRAM to store input bitstreams
- The decoder generates output video sequences in 4:2:2 color component formats

The MPEG-2 Multi-stream Decoder achieves extremely high performance when the Arrix FPOA is paired with a companion FPGA. The Arrix FPOA is optimized to perform the algorithmic functions that make up the bulk of the decoder at an input rate of 200 Mbps. The Variable Length Decoder module is provided in synthesizable VHDL that can be targeted to the companion FPGA.

Functional Overview

The functional block diagram of this decoder is depicted below.



The decoder is self-configuring and scans the incoming data stream for a variety of MPEG-2-compliant profiles and levels as shown below.

	Main	4:2:2
High 1920x1080	1 Channel Up to 90 Mbps	1* Channel Up to 200 Mbps
High 1440 1440x1080	2 Channels Up to 60 Mbps each	1* Channel Up to 200 Mbps
Main 720x576	8 Channels Up to 25 Mbps each	4* Channels Up to 50 Mbps each or 6 Channels Up to 25 Mbps each
Low 352x288	8 Channels Up to 4 Mbps each	8 Channels Up to 25 Mbps each

* The Arrix FPOA supports 6 channels of 4:2:2 format, independent of bit rate, however the FPGA limits the incoming bitstream to 200 Mbps.

Estimated Utilization

The following table summarizes the estimated resources required for the MPEG-2 Multi-channel Decoder core.

Variable/parameter	Value
FPOA target device	MathStar Arrix MOA2400D-08 FPOA
FPOA clock frequency	800 MHz
FPOA resource utilization	Approx. 320 core objects
Companion FPGA target device	Altera or Xilinx low-end FPGAs

Support

The MPEG-2 Multi-stream Decoder core for the Arrix FPOA is warranted against defects for one year from purchase. Twelve months of phone and email technical support are included.

Verification Environment

Mentor Graphics Visual Elite™ (available from MathStar) and ModelSim SE (available from Mentor Graphics).

Deliverables

The MPEG-2 Multi-stream Decoder core for FPOA includes the following components.

- Cycle-accurate, bit-true simulation model for Visual Elite simulator
- Testbench
- OHDL files
- Mapping files for MathStar's COAST tool
- Synthesizable VHDL for VLD Kernel Decoder, VBV Buffer Controller, Header Decoder and Bus Interface
- Architecture guide
- Design guide

Ordering Information

The MathStar MPEG-2 Multi-channel Decoder for FPOA is available as part number MIP-M2D02-P12. For further information, contact MathStar, Inc. at info@mathstar.com

MPEG-2 Multi-stream Decoder for FPOA. Revision 2.7

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