



## Features

---

- Supports Main and 422P profiles with bit rates from 2 Mbps to 100 Mbps
- Supports 4:2:2 and 4:2:0 color at 8 bits per color component
- Encodes at High Level (high definition) and Main Level (standard definition) resolutions
- Supports high definition 1080i @ 60 fields/sec (30 frames/sec), 720p @ 60 frames per second
- Supports High Quality I-frame only and I/P Long GOP modes
- Exhaustive motion estimation full search across range [H-8/+7, V-7/+6] and 1 reference frame to ½ pel resolution
- Accepts 4:4:4 or 4:2:2 YCbCr that is user selectable
- Variable and constant bit rate, user programmable.
- Accepts a single channel of compressed AC3 audio data format via a S/PDIF interface as defined in IEC61937
- Selectable output stream for either Elementary video, ATSC compliant transport, or program stream
- Accepts user data such as closed captioning and content advisory descriptor data
- Configurable program number and PID for video and audio
- Designed to meet ISO/IEC 13818-1 and 13818-2 requirements
- Provides runtime monitoring of PSNR and bitrate
- Provides reconstructed video in real-time through either a display device or a Gigabit Ethernet port

## Applications

---

- Professional video
- Video Servers
- Encoder boards

## Arrix FPOA Overview

---

The MathStar Field-Programmable Object Array (FPOA) architecture comprises an array of silicon objects, each performing a specific function at data rates up to 1 GHz. The architecture supports three kinds of 16-bit core objects: an Arithmetic Logic Unit (ALU), a Multiply-Accumulator (MAC) and a Register File (RF). The objects are interconnected by a two-tier interconnect structure. The interconnect structure allows for 1 GHz connectivity between Nearest Neighbor connections as well as 1 GHz connectivity between non-adjacent objects through patented Party Line interconnects. These objects are coupled with distributed internal RAM (IRAM), dedicated external memory controllers (XRAM) and a wide range of high-speed and general-purpose I/O (GPIO) to form the complete FPOA architecture. Because of its high performance, an FPOA can run many applications up to four times faster than high end FPGA architectures.

## General Description

---

MPEG-2 Encoder for FPOA core can be used to implement ISO/IEC 13818-1 / 13818-2 compliant encoders with transport stream output. The core is capable of encoding a 1080i or 720p video stream in real-time.

This encoder accepts input video streams through its high-speed I/O interface and performs the following operations:

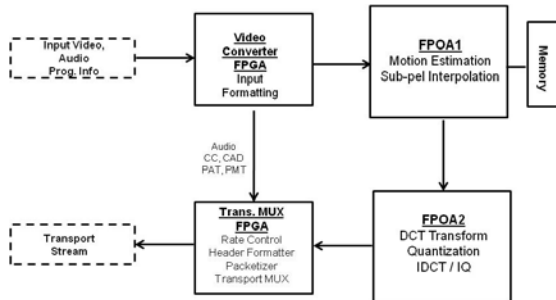
- In a P frame the encoder performs a exhaustive search across a 16x14 search window for a best match and reconstructs the motion compensated frame
- Performs DCT transform, quantization and run length encoding on all frames

- Programmable constant video bit rate between 2 and 100 Mbps
- Forwards compressed streams and control/ status commands to a host interface

The MPEG-2 Encoder with Transport Stream is implemented on an Arrix FPOA platform together with companion FPGAs. The Arrix FPOA is optimized to perform the algorithmic functions that make up the bulk of the encoder.

## Functional Overview

The functional block diagram of the MPEG-2 Encoder with Transport Stream is depicted below.



The encoder can be configured to encode a variety of input video streams at the MPEG-2 profiles and levels shown below.

Profile	YCrCb Color	HD Format
Main	4:2:0 or 4:2:2	720p@24, 30 or 60
Main	4:2:0 or 4:2:2	1080i @ 30
422P	4:2:2	720p@24,30, or 60
422P	4:2:2	1080i@30

## Estimated Utilization

The following table summarizes the estimated resources required for the core.

Variable/parameter	Value
FPOA target device(s)	FPOA1: Arrix MOA2400D-08 FPOA2: Arrix MOA2400D-06
FPOA clock frequency	FPOA1: 800MHz FPOA2: 600 MHz
FPOA resource utilization	Approx. 63% utilization
Companion FPGA target devices	Altera or Xilinx low-end FPGAs

### MPEG-2 Encoder for FPOA Revision 1.2

Notice: The information in this document is preliminary and is subject to change without notice.  
© 2006-2008 MathStar, Inc. All rights reserved.  
The MathStar name, logo, and Arrix are registered trademarks of MathStar, Inc.  
Other trademarks are the property of their respective owners.

## Support

The MPEG-2 Encoder core for the Arrix FPOA is warranted against defects for one year from purchase. Twelve months of phone and email technical support are included.

## Verification Environment

Mentor Graphics Visual Elite™ (available from MathStar) and ModelSim SE (available from Mentor Graphics).

## Deliverables

The MPEG-2 Encoder with Transport Stream core for FPOA includes the following components.

- Cycle-accurate, bit-true simulation model for Visual Elite simulator
- Testbench
- OHDL files
- Mapping files for MathStar’s COAST tool
- Synthesizable VHDL for input formatting, Huffman/VLE, rate control, header formatting, packetizing, and transport stream blocks.
- Architecture guide and Design guide

## Ordering Information

The MathStar MPEG-2 Encoder with Transport Stream for the FPOA is available as part number MIP-M2E02-P12-02. For further information, contact MathStar, Inc. at [info@mathstar.com](mailto:info@mathstar.com)