



PRESS RELEASE

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FOR IMMEDIATE RELEASE

MathStar, Inc. Announces High Definition MPEG-2 Encoder IP Core for the Arrix™ FPOA

HILLSBORO, Ore., August 7, 2007 – MathStar, Inc. (NASDAQ: MATH), a fabless semiconductor company specializing in high-performance programmable logic, announced today the availability of the company’s high definition MPEG-2 Encoder IP Core for the Arrix field programmable object array (FPOA). The intellectual property (IP) core supports high definition 720p resolutions at 60 frames per second as well as all standard definition formats. MathStar’s MPEG-2 Encoder IP Core was co-developed with Adaptive Micro-Ware, a leader in video technology solutions and a member of MathStar’s Certified Design Center (CDC) program.

“MathStar has made a substantial investment in porting broadcast video applications to the Arrix FPOA,” said Dan Sweeney, MathStar COO. “The FPOA offers performance above and beyond other programmable logic products, which makes it ideal for high-definition video processing. The combination of Adaptive Micro-Ware’s video expertise and the Arrix FPOA’s 1 gigahertz deterministic timing enable a very high-end MPEG-2 encoder feature set on a low cost platform.”

“MathStar’s Arrix FPOA allowed Adaptive Micro-Ware to develop the MPEG-2 encoder IP core in a short amount of time.” said Bob Kniskern, president of Adaptive Micro-Ware. “By combining the FPOA architecture with inexpensive FPGAs, we were able to target a best-in-class feature set including extensive motion estimation, a low constant bit-rate and very high picture quality – all on a re-programmable platform.”

According to Kniskern, Adaptive Micro-Ware first selected the FPOA for work with a major telecommunications customer that needed a higher-performance form of programmable logic to help compress video for storage and distribution over the Internet. Since then, the company has been able to leverage this investment into design services contracts with other firms.

The MPEG-2 Encoder IP Core is part of MathStar's Pro Video Library, which also includes MPEG-2 Multi-Stream Decoder and JPEG-2000 Encoder IP Cores as well as a roadmap to MPEG-4/H.264 IP. The MPEG-2 Encoder IP is scalable across one or two FPOA devices, depending on the level of compression required. The IP core will also be enhanced to support 1080i formats before the end of the year. For pricing and availability of the MPEG-2 Encoder IP Core, please contact MathStar at www.mathstar.com.

About MathStar, Inc.

MathStar is a fabless semiconductor company offering best in class, high-performance programmable logic solutions. MathStar's field programmable object array (FPOA) can process arithmetic and logic operations at 1 gigahertz clock rates, which is up to four times faster than even the most advanced FPGA architectures in many applications. MathStar's Arrix family of FPOAs are high-performance programmable solutions that enable customers in the machine vision, high-performance video, medical imaging, security & surveillance and military markets to rapidly and cost effectively innovate and differentiate their products. FPOAs are available now and are supported by development tools, IP libraries, application notes and technical documentation. For more information, please visit <http://www.mathstar.com/>.

Statements in this press release, other than historical information, may be "forward-looking" in nature within the meaning of Section 21E the Private Securities Litigation Reform Act of 1995 and are subject to various risks, uncertainties and assumptions. These statements are based on management's current expectations, estimates and projections about MathStar and its industry and include, but are not limited to, those set forth in the section of MathStar's Annual Report on Form 10-K filed with the Securities and Exchange Commission on March 31, 2006 under the heading "Risk Factors." MathStar undertakes no obligation to update any forward-looking statements in order to reflect events or circumstances that may arise after the date of this release.

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